ABSTRACT

In one aspect, the present invention features a method of manufacturing an integrated circuit package including providing a substrate having a first surface, a second surface opposite the first surface, a cavity through the substrate between the first and second surfaces and a conductive via extending through the substrate and electrically connecting the first surface of the substrate with the second surface of the substrate, applying a strip to the second surface of the substrate, mounting a semiconductor die on the strip, at least a portion of the semiconductor die being disposed inside the cavity, encapsulating in a molding material at least a portion of the first surface of the substrate, and removing the strip from the substrate. In another aspect, the invention features an integrated circuit package including a substrate having a first surface, a second surface opposite the first surface, a cavity through the substrate between the first and second surfaces and a conductive via extending through the substrate and electrically connecting the first surface of the substrate with the second surface of the substrate, a semiconductor die electrically coupled with the conductive via, at least a portion of the semiconductor die being disposed inside the cavity of the substrate, an encapsulant material encapsulating a portion of the semiconductor die such that at least a portion of a surface of the semiconductor die is exposed.